**What is claimed is:**

1. A test device for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors, wherein the test device is disposed in a scribe line region of a wafer, comprising:

parallel first and second memory cell structures disposed in the scribe line region, each having a deep trench capacitor and a transistor structure;

an active area disposed between the first and second memory cell structures, wherein the active area overlaps the first and second memory cell structures a predetermined width; and

first to fourth conductive pads disposed on both ends of the first and second memory cell structures respectively.

2. The test device as claimed in claim 1, wherein a first resistance is measured by the first and second conductive pads disposed on both ends of the first memory cell structure, and a second resistance is measured by the third and fourth conductive pads disposed on both ends of the second memory cell structure, and alignment shift ($\Delta W$) of the active area and the first and second memory cell structures is estimated according to the first resistance, the second resistance, and the predetermined width.

3. The test device as claimed in claim 2, wherein the alignment shift ($\Delta W$) is estimated according to an equation of $\Delta W = W \times \frac{(R2 - R1)}{(R2 + R1)}$;

wherein R1 is the first resistance, R2 is the second resistance and W is the predetermined overlap width between the active area and the first and second memory cell structures respectively.

4. The test device as claimed in claim 1, wherein the first to fourth conductive pads are made of polysilicon.

5. The test device as claimed in claim 1, wherein the wafer further has a memory region including a plurality of memory cells with vertical transistors.

6. A method for detecting alignment of deep trench capacitors and word lines in DRAM devices with vertical transistors, comprising:

providing a wafer with at least one scribe line region and at least one memory region;

forming a plurality of memory cells with vertical transistors in the memory region and at least one test device in the scribe line simultaneously with the same masks and process, the test device including:

parallel first and second memory cell structures disposed in the scribe line region, each having a deep trench capacitor and a transistor structure;

an active area disposed between the first and second memory cell structures, wherein the active area overlaps the first and second memory cell structures a predetermined width; and

first to fourth conductive pads disposed on both ends of the first and second memory cell structures respectively;

detecting a first resistance between the first and second conductive pads disposed on both ends of the first memory cell structure, and a second resistance between the third and fourth conductive pads disposed on both ends of the second memory cell structure;

determining alignment of the active area and the first and the second memory cell structure according to the first resistance and the second resistance; and

determining alignment of the active area and the memory cells in the memory regions according to alignment of the active area and the first and the second memory cell structures of the test device.

7. The method as claimed in Claim 6, further comprising a step of determining alignment shift (Δw) of the active area and the first and the second memory cell structures according to the first resistance, the second resistance, and the predetermined width between first and second memory cell structures and the active area respectively.

8. The method as claimed in Claim 7, wherein the alignment shift (ΔW) is estimated by an equation:

$$\Delta W = W \times \frac{(R2 - R1)}{(R2 + R1)};$$

wherein W is the predetermined overlap width between first and second memory cell structures and the active area respectively; R1 is the first

resistance between the first and second conductive pads disposed on both ends of the first memory cell structure; and R2 is the second resistance between the third and fourth conductive pads disposed on the second memory cell structure.